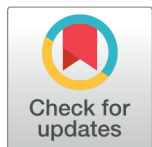


Bottom-up and Top-down Strategies for Fabrication of Silicon Nanowires



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Silicon (Si) is an important technological material with widespread applications, especially in electronics and optoelectronics. Due to its specific bandgap and low light absorption coefficient, the efficiency of Si-based photodetectors and solar cells is not sufficient for growing industrial needs. By patterning Si into nanowire structures, not only the light-trapping efficiency of the Si can be increased for solar cell and photodetector applications, but the process also imparts other functionalities to nanowires suitable for applications such as antibacterial surfaces, sensing, batteries, etc. Large scale applications of Si nanowires depend on their scalable fabrication. In this article, we summarize the most commonly used fabrication techniques for Si nanowires and discuss their advantages and disadvantages.

Keywords: Silicon, Nanowires, Bottom-up, Growth, Top-down

INTRODUCTION

Silicon is a material that offers qualitative solutions to the recent technical problems of the modern world by its wide spectrum of applications in numerous areas. Especially, in electronic and photovoltaic (PV) industries the strong domination of Si is highly related to its advantageous properties. One of the most important points is its abundance on earth, ensuring the availability of large single crystals with high purity. Besides, having benign thermal and mechanical properties, superior opto-

electronic properties of Si provide numerous applications in energy conversion technology. The bandgap of Si, 1.1 eV, matches with the visible spectrum. Thus, it lies in the optimum range in the solar spectra to harvest solar energy. Hence, silicon is the prior element in the photovoltaic industry and 90% of the solar cells employed in solar energy conversion technology are based on Si today.¹ However, having indirect bandgap nature which leads to losses in absorption and emission of light is a significant drawback of silicon PVs. Also, relatively low absorption in the solar spectra requires a

thicker Si layer. Therefore, the optical properties of Si should be improved and this can be accomplished by the implementation of Si nanostructures. Similarly, developments in information technology can be observed by employing materials that show a high transmission rate and low heat dissipation. These material features can also be realized by Si nanostructures. Silicon nanowires (SiNWs) have been investigated extensively to fabricate high-quality devices by using cost-effective approaches. Research on SiNWs mostly focused on the optimization of the structural properties including morphology, size of the wires, or array periodicity. In addition, both theoretical and experimental studies have been carried out on the optical and electrical properties of SiNWs.² SiNWs have found applications in electronics, photovoltaics, sensing and as antibacterial surfaces.^{3–6} In traditional Metal-Oxide-Semiconductor Field-Effect-Transistors (MOSFET), SiNWs act as thin channel material. These NW based FETs are excellent candidates for scaling down the transistors, and they also outperform their bulk counterparts in terms of off-state leakage current and drive current generation per device, and low-frequency noise.^{7,8} In Photovoltaics, due to better light trapping at comparatively lower thickness, and the possibility of making radial p-n junctions not only drastically reduces the cost but also increases the efficiency.^{9–11}

The scope and potential of the above-mentioned application of SiNWs depend on the large scale production of high-quality SiNWs. The Quality of SiNWs depends on the methods used for producing SiNWs. Several synthesis methods have been studied for SiNWs fabrication and hence there are various well-established growth techniques that have already been developed. The growth of nanostructures on Si surfaces can be both obtained by bottom-up or top-down deposition techniques. Bottom-

up growth techniques are mainly based on vapor-liquid-solid (VLS) mechanism.¹² Top-down techniques include various etching techniques including HF etching¹³, reactive ion etching^{14,15}, laser ablation¹⁶, and the Fray-Farthing-Chen-Cambridge (FFC-Cambridge) process¹⁷ where electrochemical reduction of SiO₂ method is embedded, are most commonly. However, the top-down approaches employed to obtain SiNWs have been found to be more common since bottom-up techniques have some drawbacks such as slow growth rates and relatively high costs. Metal-assisted chemical etching (MACE) is a new innovative technique that is easy, scalable, cost-effective and CMOS compatible.¹⁸ metal-assisted chemical etching (MACE) and reactive ion etching (RIE) are more recent and well-established growth techniques. In this review, we will summarize these techniques and will discuss their advantage and disadvantages.

BOTTOM-UP APPROACHES FOR FABRICATION OF SiNWs

Vapor-Liquid-Solid (VLS) Growth of SiNWs

The vapor-liquid-solid growth mechanism of single crystal growth was first mentioned by Wagner and Ellis in their paper of the same name. In this study, they obtained silicon nano-whiskers by VLS growth mechanism.¹⁹ In VLS growth, SiNWs are fabricated with the help of a vapor phase precursor and a liquid phase catalyst and directional nucleation of the Si material in the form of wires provided. Therefore, this deposition technique relies on three different stages, namely alloying, nucleation, and wire growth². The first stage is the formation of metal nanoparticles on a silicon surface. Typically, gold (Au) is used as metal droplets in this process and the formation of Au nanoparticles can be provided by lithography

or self-assembly¹. During the SiNW growth process, the background Si flux is provided by vapor phase precursor, for instance, silane (SiH₄), by using methods such as chemical vapor deposition, electron-beam evaporation, or molecular beam epitaxy. Then, the system is heated up to temperatures above the Au–Si eutectic point. When the supersaturation point of the droplet is reached by the background Si flux, the nucleation of the solid Si in the interface between Si and the droplet starts.¹⁷ As a result, the growth of nanowires takes place vertically and the Au droplets are pushed up.¹ The VLS growth process is presented schematically in Figure 1.

Silanes and chlorosilanes are the most commonly used Si precursors for VLS growth Si NWs. Chlorosilanes usually crack at higher temperatures so growth will be high temperature (800–1000°C). As silane usually decomposes at low temperatures, VLS growth can happen at relatively low temperatures (400–600 °C). However, silanes are explosive in nature, so great care needs to be taken while handling these materials.

Au is the most commonly used catalyst due to its easy availability, non-toxicity, and low temperature eutectic with comparably high Si solubility. However, the cost and the fact that Au act as a deep level impurity in the Si can seriously affect the carrier transport of the Si nanowires. In addition to Au, other catalysts such as Ag, Al, Bi, Cd, Co, Cu, Dy, Fe, Mg, Pr, Pt, Ru, Sn, Te, Mn, Ni, Ga, Gd, In, Os, Pb, Pd, Ti, and Zn, can also be used as a catalyst during the VLS process.^{21–39} Catalysts can be divided into type-A (Au like with single eutectic point), type-B (have much lower solubility of Si and a single eutectic point), and type-C (which are silicide forming metals). The classification of metals is shown in Figure 2. The energy level of Au and other metals catalysts used for the growth of SiNWs and their growth temperatures are given in Figure 3.

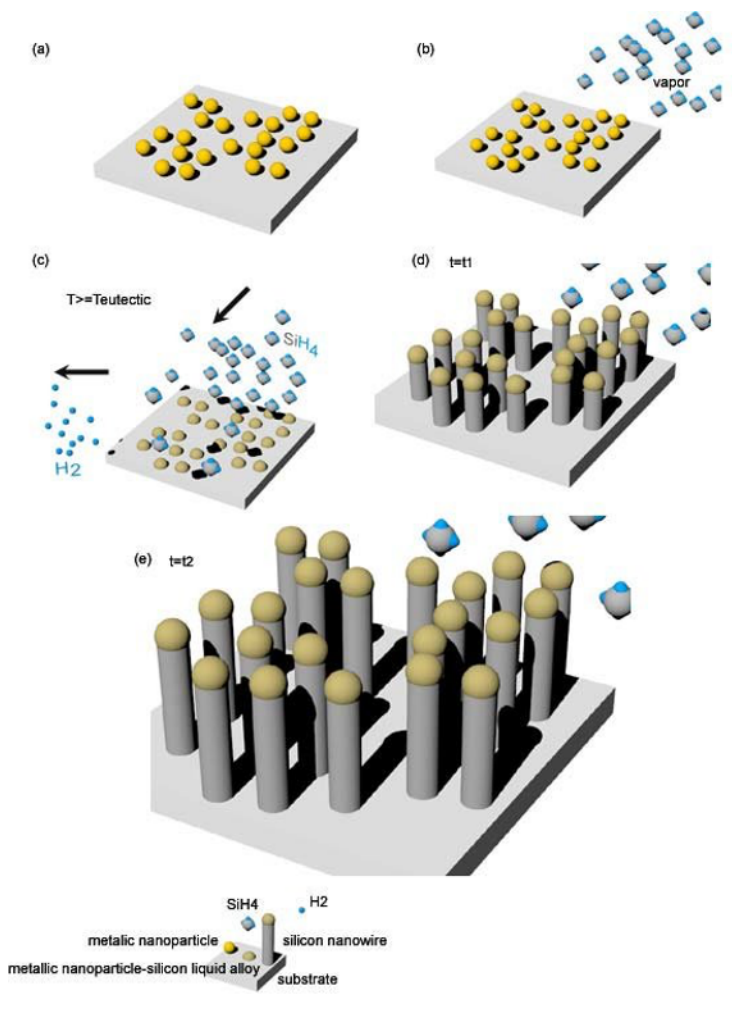


Figure 1. The VLS process for silicon nanowire synthesis.²⁰

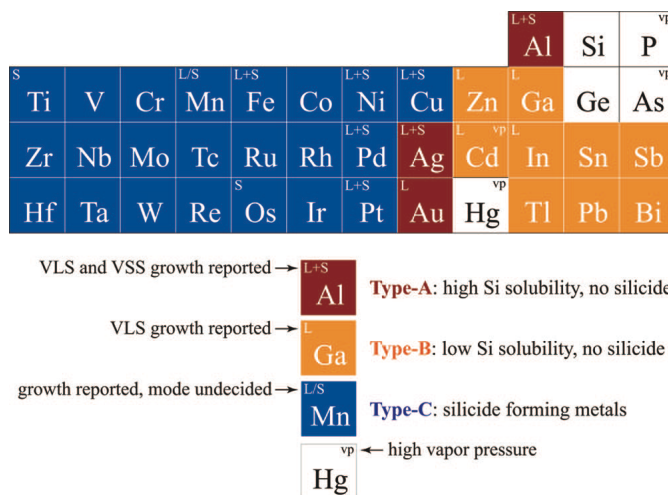


Figure 2. Metals classified based on their phase diagram and their position in the periodic table.²¹ Adapted with permission from reference 21. Copyright 2018 American Chemical Society.

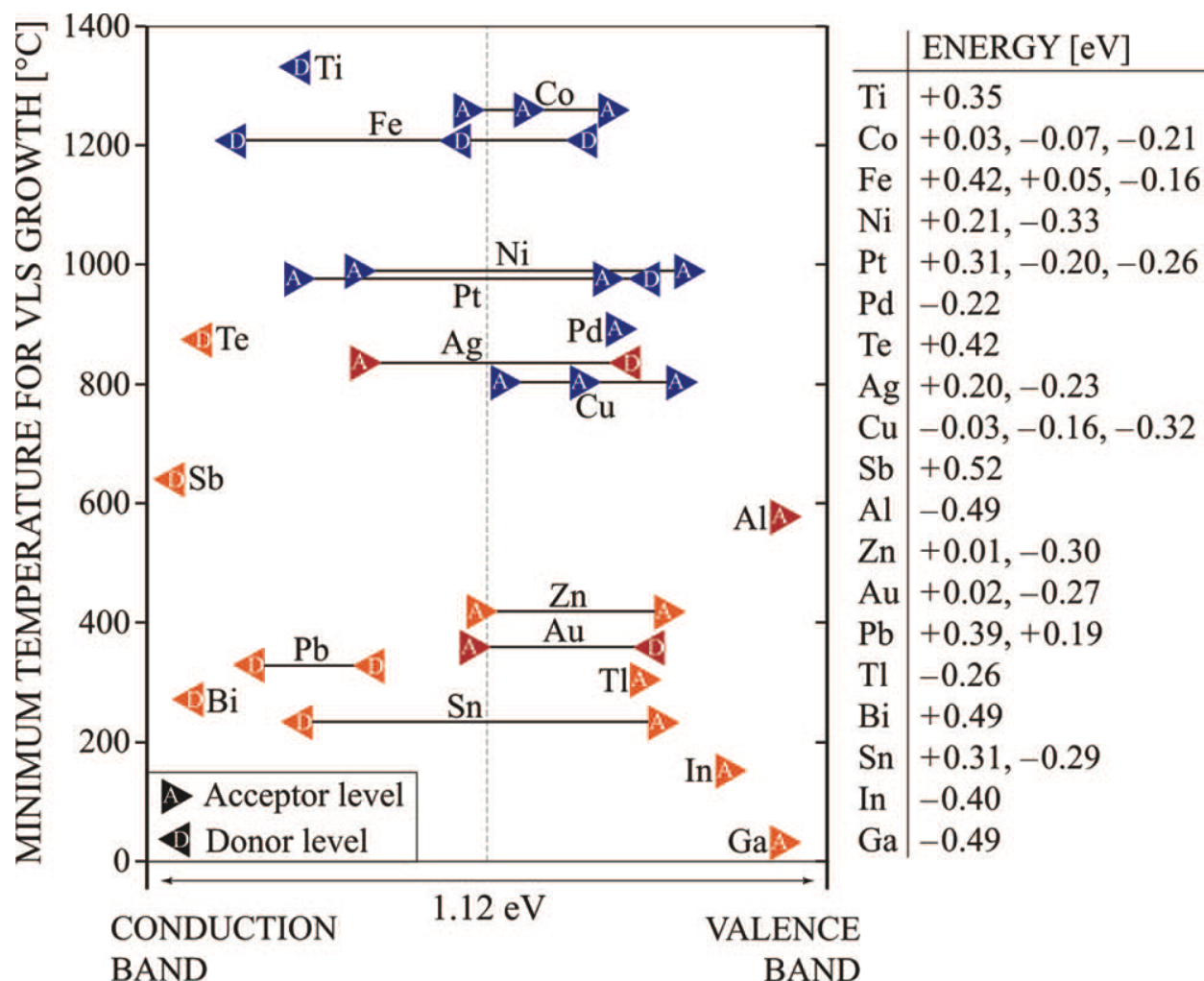


Figure 3. The minimum temperature required for metal catalysts to grow SiNWs by vapor-liquid-solid (VLS) method is plotted against their respective impurity energy level in Si.²¹ The colour codes are adopted from Figure 2: Adapted with permission from reference 21. Copyright 2018 American Chemical Society.

There are multiple VLS techniques, which include high temperature chemical vapor deposition, low-temperature chemical vapor deposition, supercritical-fluid-based, solution-based, molecular beam epitaxy, laser ablation, and silicon monoxide evaporation based. These techniques differ mainly on how the silicon is fed. Si is either fed as elemental Si or a Si compound. Each technique has its advantages and disadvantages, which are discussed elsewhere.²¹ Chemical vapor deposition is generally the preferred technique, as it offers morphological control, versatility and control over electrical properties. However, issues

related to kinking and growth orientation need to be solved.

TOP-DOWN APPROACHES FOR FABRICATION OF SiNWs

Reactive Ion Etching

Reactive ion etching is a top-down approach and perhaps its biggest advantage is its CMOS compatibility. It's a dry etching technique and is different from chemical etching. It uses chemically reactive plasma to etch Si to obtain desired patterns. A strong

radio frequency (RF) electromagnetic field generates the plasma of a reactive gas. Electrons in the plasma are being accelerated and some of the accelerated electrons will sit on Si surface, making it more electron-rich which helps attract the reactive plasma ions to the Si substrate. These plasma ions will react with Si and etch it. Oxygen or halogens (F, Cl, etc.) are generally used as plasma species and the reactivity of the plasma increases with the electronegativity of these halogens. SF₆ or chlorine (Cl₂) gas is generally used as a plasma source and C₄F₈ is used as passivation gas to enhance the anisotropic effect. Once the Si surface

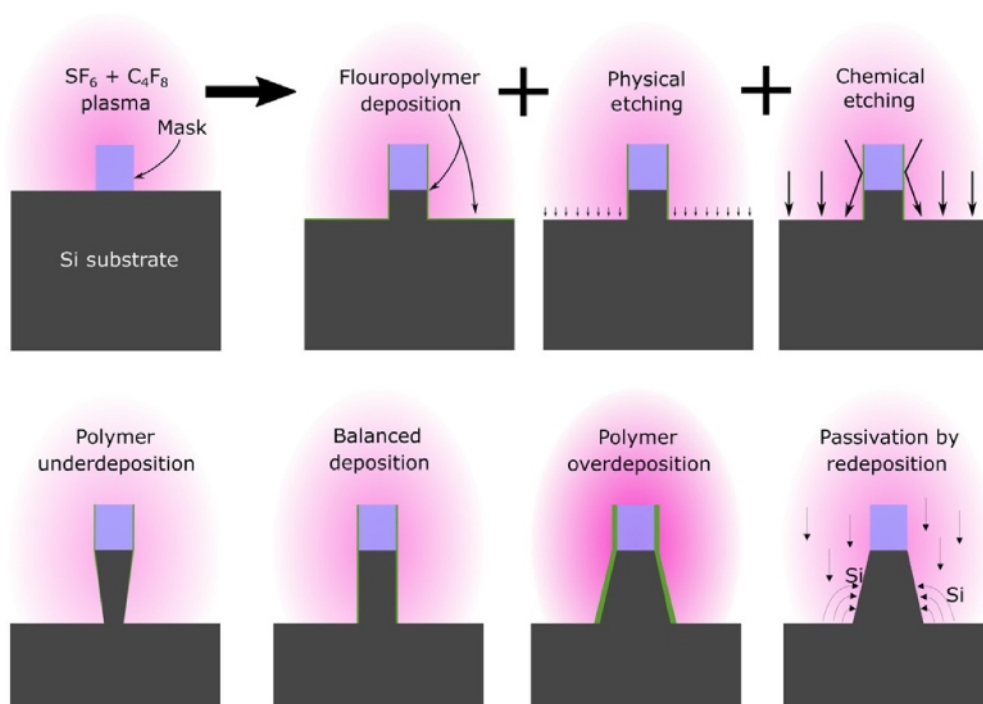


Figure 4. The top panel shows schematics of RIE process. The bottom panel shows the Influence of over/under passivation and redeposition on etch profile (bottom).⁴⁰ Adapted with permission from ref 40. Copyright 2018 Elsevier.

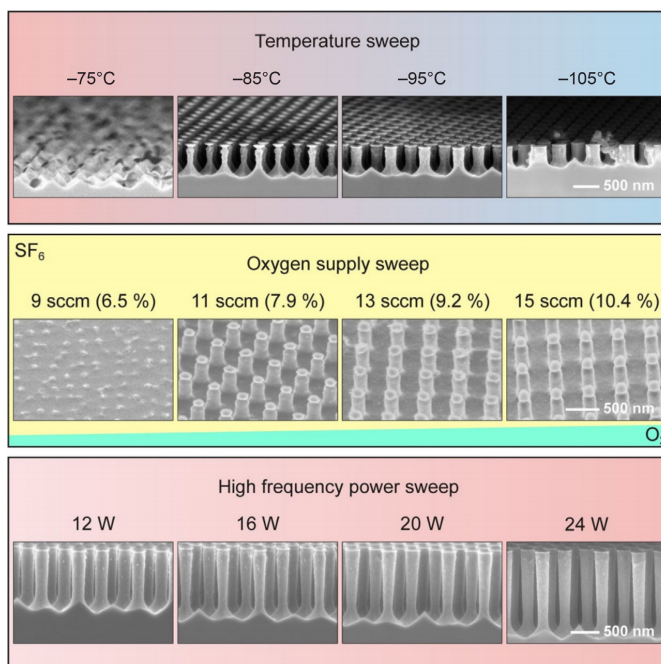


Figure 5. Overview of the effect of etching parameters (temperature, oxygen content, and plate bias) on the morphology of SiNWs.⁴¹ Adapted with permission from ref 41. Copyright 2014 Springer.

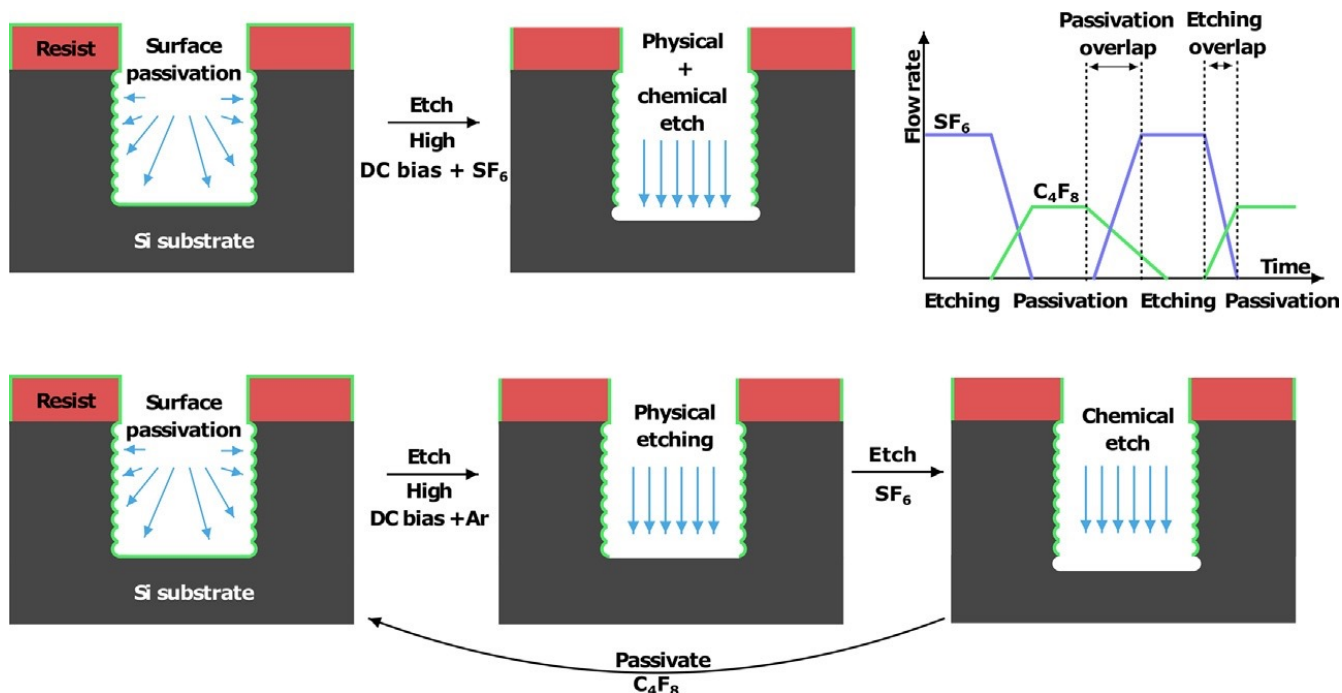


Figure 6. Schematic of a two-step (top) and three-step Bosch etching process (bottom).⁴⁰ Adapted from ref 40. Copyright 2018 Elsevier.

is passivated, chemical etching can't take place anymore. To continue the etching process, the bottom surface of the passivated surface is bombarded with energetic ions, which removes the protective passivation layer and allows further chemical etching. To increase the anisotropy, a bias is also applied to Si to direct the ions to the bottom of the sample. During the etching process, by-products will release, which in some cases, redeposit on the Si nanowire, and cause serious morphological changes (Figure 4). Under or over deposition of the passivation layer can also affect the morphology of the SiNWs.

The morphology of SiNWs can be fine-tuned by changing the gas plasma, temperature, substrate bias, flow rate, and plasma power. Figure 5 shows the effect of various parameters on SiNW growth. Details on the effect of these parameters can be found elsewhere.⁴¹

In RIE, passivation, physical etching and chemical etching take place at the same time, as shown in Figure 4. A particular example of RIE is deep reactive ion etching (DRIE) or the Bosch

process, where passivation, physical, and chemical etching steps take place on a different time scale. DRIE process alternates repeatedly between the etching and passivation process, and involves, physical etching, chemical etching and passivation steps. Bosch process can be two or three-step (Figure 6)

Si, are Ti, Cr, even polystyrene particles^{42,43} are generally used as masks during the etching. DRIE process allows the fine-tuning of the physical etching process, which does not damage the mask, and hence, SiNWs with better control over diameter can be easily obtained. Generally, DRIE process is suitable for etching long nanowires with a smaller diameter. However, one drawback associated with DRIE is scalloping. Sequential etching and passivation steps give rise to undercuts which is the main reason for scalloping. Scalloping leads to rough surfaces, hence technique is not suitable for applications, where smooth surfaces are required.

To reduce the scalloping, SiNWs of larger diameter are first prepared by the DRIE, and their surface is oxidized. Afterwards, the top SiO₂ layer is etched away chemically with HF to produce smoother and lower diameter SiNWs. To further enhance the control over the morphology of SiNWs and achieve smaller diameter SiNWs, DRIE has been coupled with state of the art lithography techniques including UV, electron beam, X-ray and nanoimprint lithography.^{44–46}

Metal Assisted Chemical Etching (MACE)

MACE is the wet chemical etching of semiconductors, especially Si, in the presence of metal catalysts. The etching and its effects on the Si substrates are well-known procedures since it is commonly applied in the industrial production of Si-based devices. However, MACE is a relatively new technique, and though it has great potential for its future use in the industry, currently, its applications in the Si etching in the

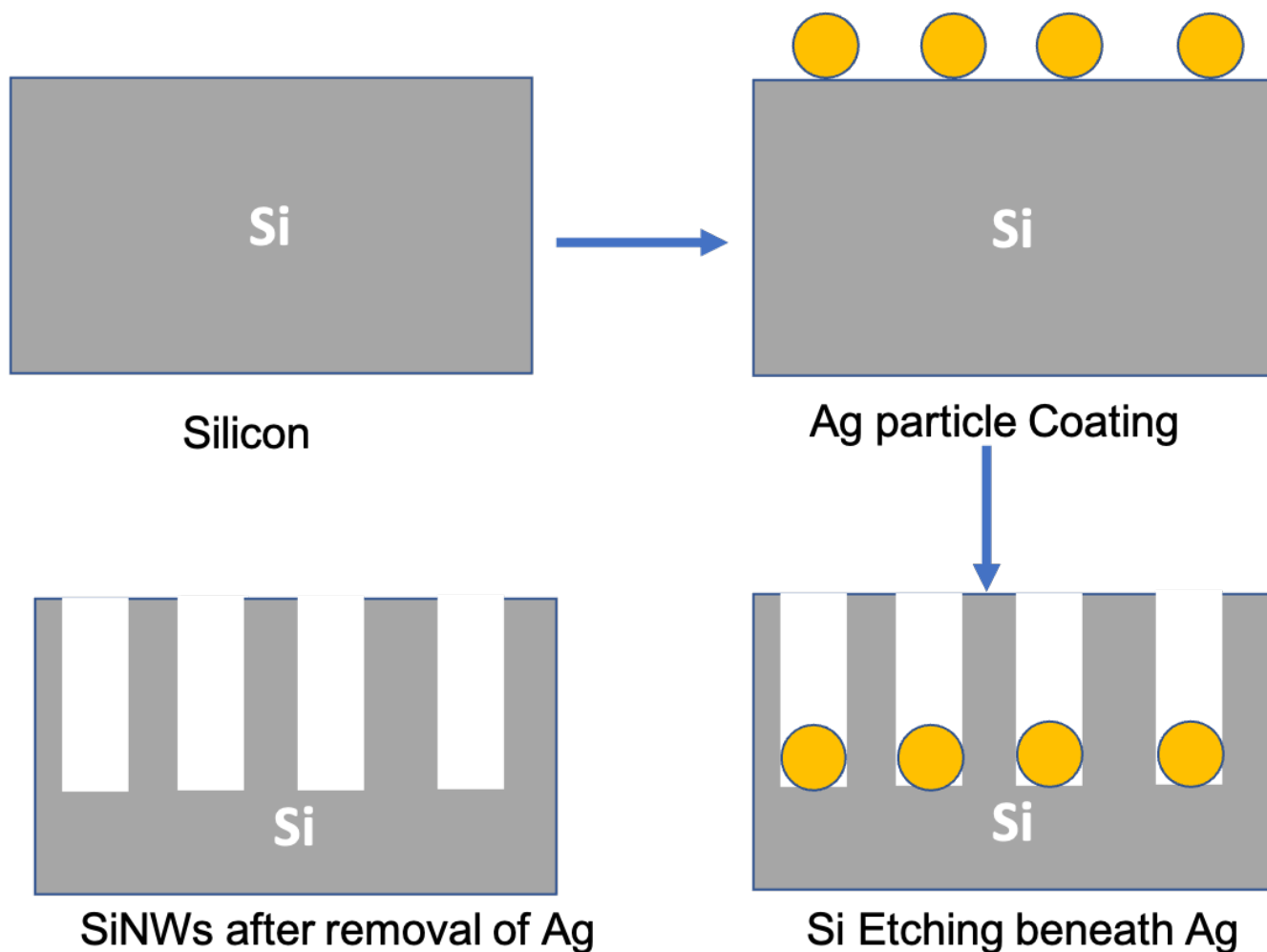


Figure 7. Schematics of MACE fabrication of SiNWs.

industry are limited. Similar to VLS growth, the MACE process starts with the deposition of the metal nanoparticles on the Si substrate. In addition to Au, silver (Ag) is also one of the most popular material in this stage since both Au and Ag nanoparticles can be grown by a wide range of deposition techniques such as thermal evaporation, sputtering and electron beam evaporation, etc. Other metals that can be used as catalyst include platinum, palladium, aluminum, iron, nickel, and copper. Metals are deposited on the Si surface using variety of methods including sputter deposition, electron beam evaporation, thermal evaporation, electroless deposition, focused ion

beam assisted deposition, etc. Some of these methods can be combined with lithography to selectively cover Si regions with the metal. Each method has its own advantages and disadvantages. MACE, besides presenting the simple process, also provides the control over the deposition of catalyst with high precision.

Electroless plating is the simplest method employed for MACE process. Si substrate is immersed in HF/noble metal solutions (e.g., AgNO_3 or HAuCl_4), where deposition and etching happens simultaneously. Metal ions in the solution acquire electrons from the Si valance band and inject holes into the Si. Consequently, metal

ions are reduced and deposit on the surface as metal particles, and Si beneath these metal particle is oxidized in the form of SiO or SiO_2 . Finally, the removal of SiO and SiO_2 by HF solution results in the beginning of formation of Si nanowires. Continuous oxidation of the Si under the nanoparticles and removal of the oxide layers by HF solution leads to the sinking of the metal nanoparticles to the deeper level of the Si substrate (Figure 7). As a result, final structure contains SiNWs on the surface and metal nanoparticles embedded between them¹⁷.

Though, the light trapping efficiency of SiNWs fabricated using MACE is excellent, but the control

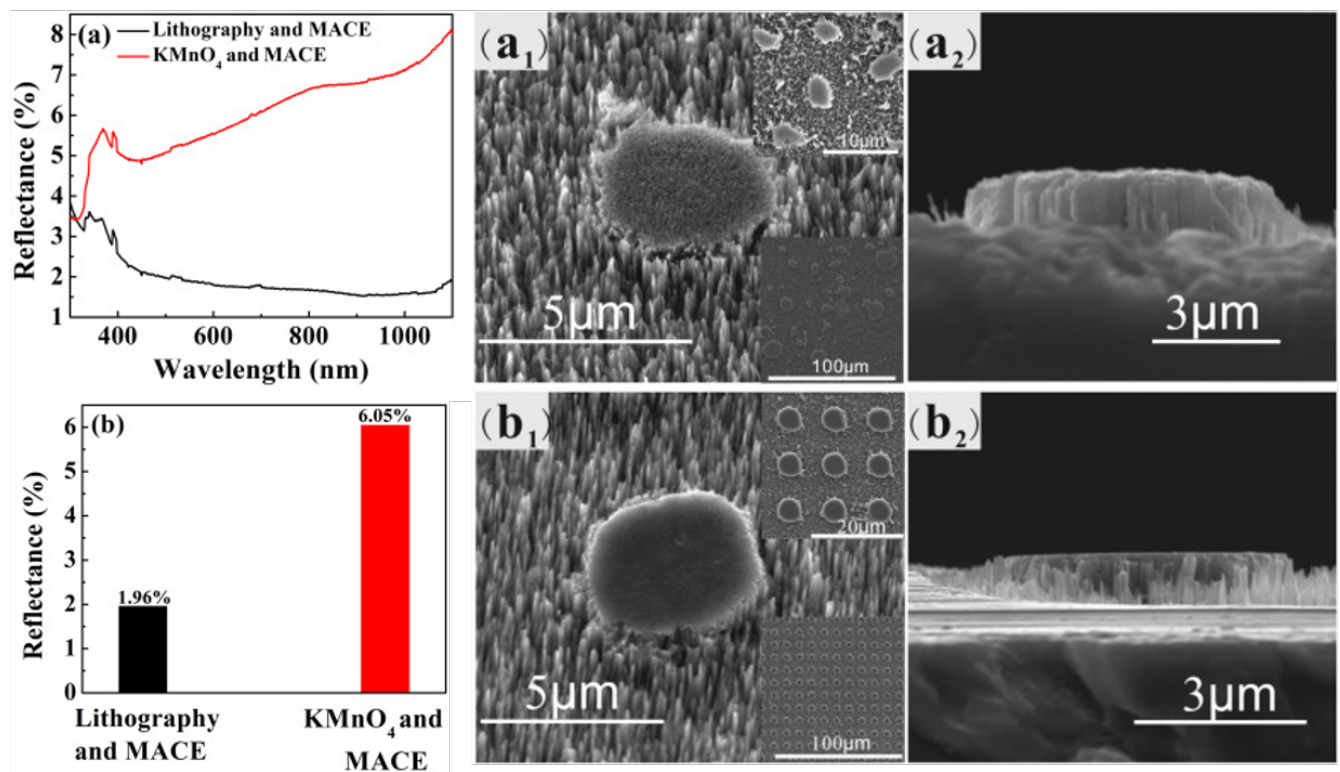
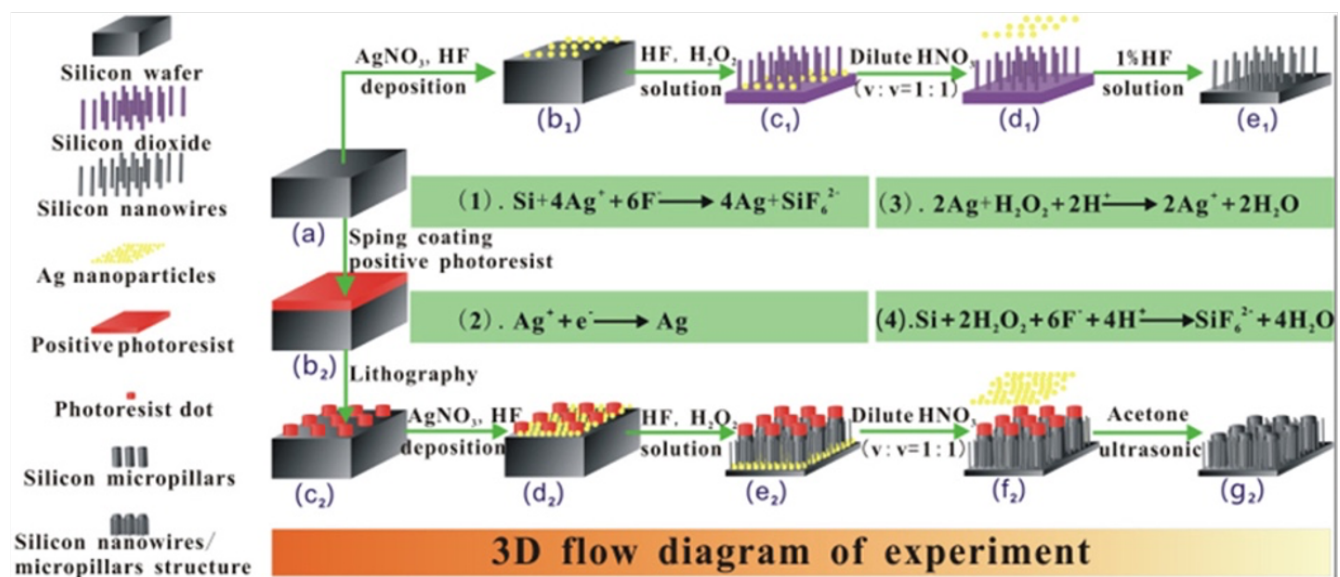


Figure 8. A synthesis scheme, reflectance spectra and SEM images of silicon nanowires/micropillars structure fabricated by using lithography and MACE.⁴⁸ Adapted from ref 48. Copyright 218 Elsevier.

over shape, density and regularity is poor. Si micropillars fabricated using more common lithography methods have excellent control over morphology, but their light-trapping efficiency is not good.⁴⁷ A combination of MACE with lithography can produce SiNWs with great control over the morphology as well as good light-trapping efficiency. Xi et al.⁴⁸ have demonstrated a facile synthesis of SiNWs/SiMPs using lithography and MACE, where they first spin-coated and baked a photoresist on the Si wafers. Photoresist dots of 5 μm diameter were obtained by exposing the photoresist for 90–100 s and subsequent development in solvent for 40–50 seconds, and then MACE method was used to grow SiNWs/SiMPs. As can be seen in SEM image of Figure 8, SiNWs/SiMPs structures were very well arranged and also showed the better light trapping efficiency.

MACE can be used in tandem with colloidal lithography for the production of large-scale homogeneous SiNW arrays (Figure 9).^{49,50} Colloidal lithography is not only simple but also a very cost-effective approach for fabricating SiNW arrays with precise control over the geometry without requiring expensive and sophisticated nanopatterning techniques. It involves the monolayer deposition of the colloidal spheres (polystyrene or core-core-shell SiO₂ particles), with controllable size (plasma etching is used to shrink the particles) and dispersion.⁵¹ While the colloidal mask can be fabricated by a variety of methods (drop-casting, spin-coating, etc.) large-scale and good quality monolayers without macroscopic defects can be only be grown by self-assembly on the water-air interface, ideally by using a Langmuir trough. This colloidal monolayer act as a template for metal deposition. After the lift-off process metal nanohole arrays are obtained which are used for subsequent MACE etching. Thus, the combination of colloidal lithography and MACE provides

a benchtop, cost-effective, and versatile way to synthesize SiNW arrays with tuneable geometries. Grain boundaries and other defects on the colloidal particles can affect the final quality of the SiNWs.

Fabricated SiNWs can be further processed to tailor their properties for any specific applications. For example, bisegmented and graded arrays have been fabricated from MACE synthesized NW arrays.⁵³ As shown in Figure 10, synthesized NW arrays were dipped into KOH solution to thin down the diameter of NWs by etching. A further MACE step grew thicker NWs at the bottom. Diameter The diameter of the top segment depended on the KOH etching, while the diameter of the bottom segment was dependent on the colloidal template. While the single-diameter NWs show a single sharp dip in their reflectance spectrum, the bisegmented NWs shows a significantly broadened reflectance dip. As can be seen for the absorption maps, the bottom large diameter segment absorbs more at longer wavelengths, while the top smaller diameter section absorbs more at shorter wavelengths. This combination is responsible for a broader dip in the reflection spectrum of bisegmented NWs.

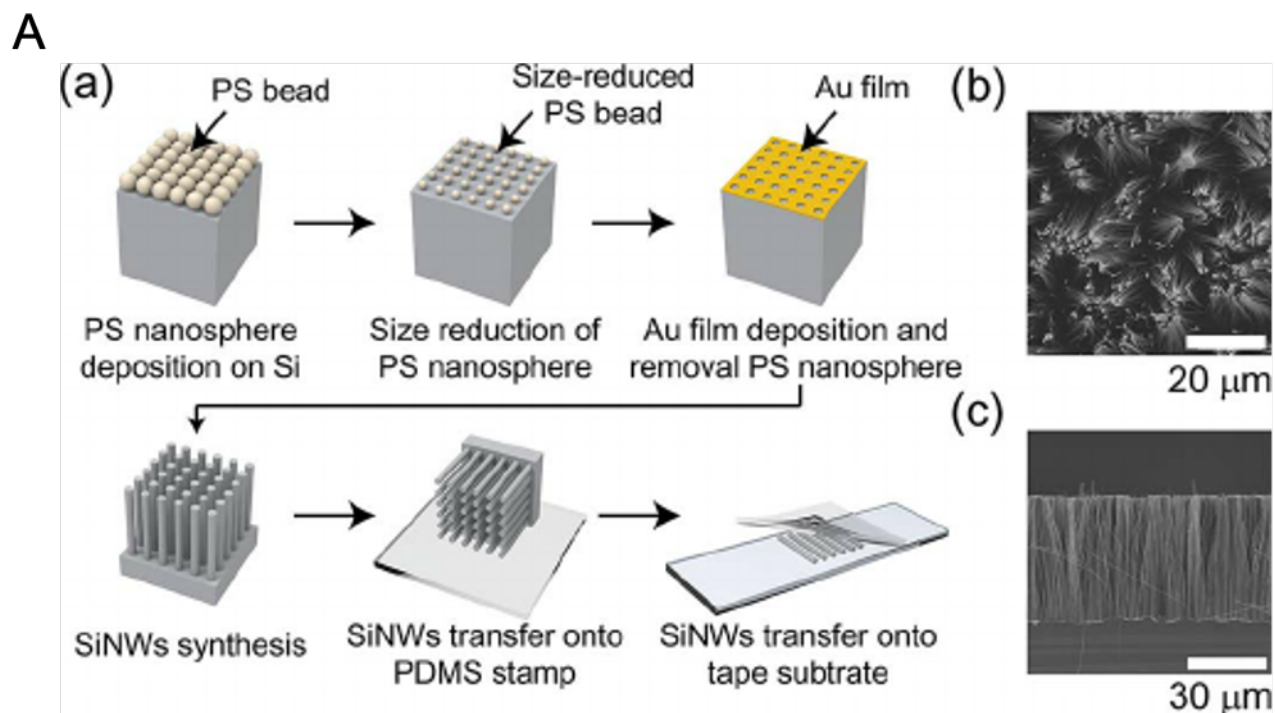
The same group fabricated graded NW arrays by dipping the MACE fabricated NWs into a two-phase mixture of KOH at the bottom and hexane at the top, see Figure 11. Progressive removal of the substrate from the solution leads to a gradual change of the NW diameter, which is also depicted by the change in colour from blue to grey. Change of colour is also reflected in the UV-Vis reflectance spectra. For homogeneous etching, hexane is used to reduce the residual KOH adhering to the SiNW substrate.

SUMMARY AND OUTLOOK

We have summarized VSL, RIE and MACE techniques for the fabrication of SiNWs (Figure 12). VLS mech-

anism is not only applicable to Si but also to a range of other materials. It is a bottom-up approach to grow SiNWs. CVD technique is the best technique to grow SiNWs via the VSL method as it offers better control over morphology and electrical properties. RIE and MACE are bottom-up approaches. Since bulk Si is used as the initial material range of SiNW shapes and morphologies can be carved into the bulk Si, a benefit not associated with bottom-up methods. Moreover, post-SiNW fabrication, leftover bulk Si can also be used depending upon the requirement of the application. RIE is a well-matured CMOS process, so, SiNW fabricated with RIE can be integrated with Si devices easily. Moreover, DRIE coupled with advanced lithographic techniques allows the fabrication of long nanowires with thin diameters. MACE is a simple, innovative and cost-effective new technique for the fabrication of large scale and integration with the CMOS process. Due to the inherent simplicity of the process, by tuning different parameters, gradient and bisegment SiNWs can also be fabricated easily. MACE can also work together with advanced lithographic techniques to give better control over size and morphology. Lesson learnt from different techniques, with a combination of different growth techniques, and coupling these fabrication techniques with advanced lithographic methods can open the way for large scale, cost-effective and high-quality SiNW growth for large scale applications such as solar cells, sensors, etc.

Apart from the techniques mentioned in this review article, there are also other less commonly fabrication techniques. For example, laser beam ablation, ion beam etching, thermal evaporation oxide-assisted growth are the top-down synthesis methods. While, molecular beam epitaxy and precipitation from solution are the examples of bottom-up strategies.



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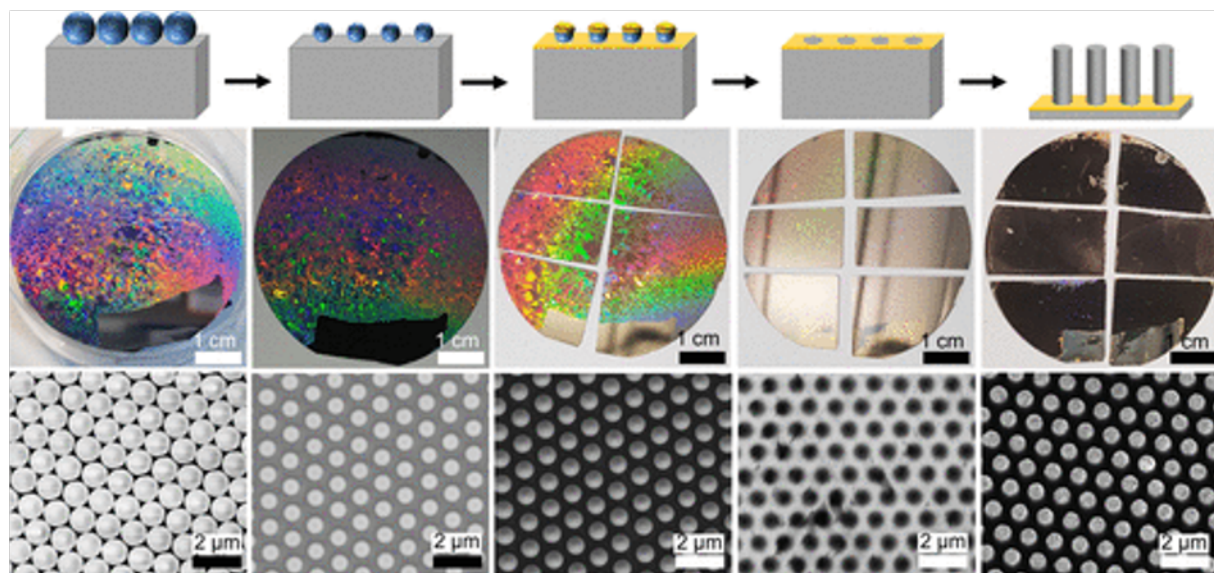


Figure 9. (A) (a) Schematic of MACE SiNW fabrication with Nanosphere Lithography. (b, c) SEM top and cross-sectional image of SiNWs, respectively.⁵¹ Adapted from ref 52. Copyright 2015 IEEE. (B) Synthesis of SiNW arrays using the combination of MACE and colloidal lithography. The top row shows the schematics of steps involved in fabrication. The middle row shows the photographs of 2" Si wafers during the process. Bottom row: SEM images at every step in top row.⁵² Adapted with permission from ref 52. Copyright 2020 American Chemical Society.

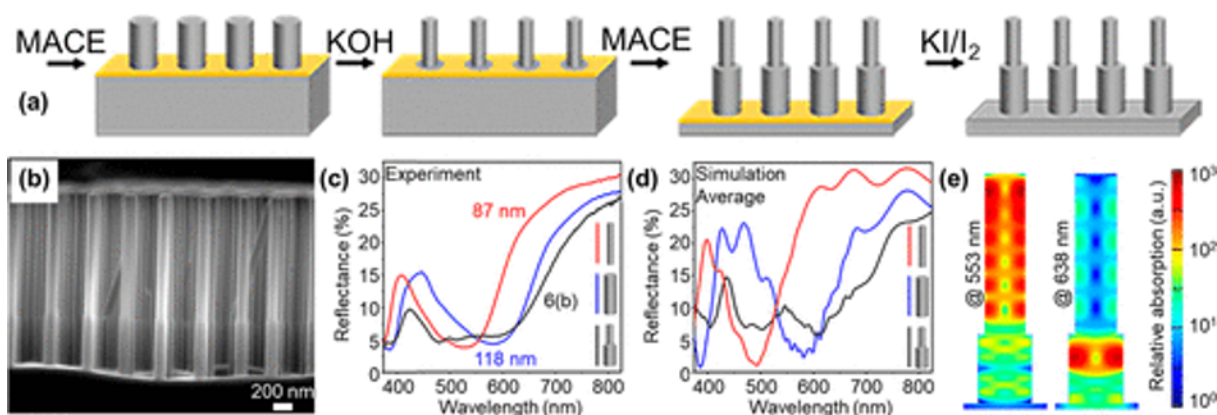


Figure 10. (a) Schematic of the synthesis of bisegmented SINW using sequential MACE and KOH etching steps. (b) Secondary electron SEM image of bisegmented SiNWs. (c, d) Measured and simulated reflectance spectra of two different and bisegmented NWs, respectively. (e) Two-dimensional maps of the simulated relative absorption of bisegmented SiNWs at 553 and 638 nm.⁵³ Adapted with permission from ref 53. Copyright 2020 American Chemical Society.

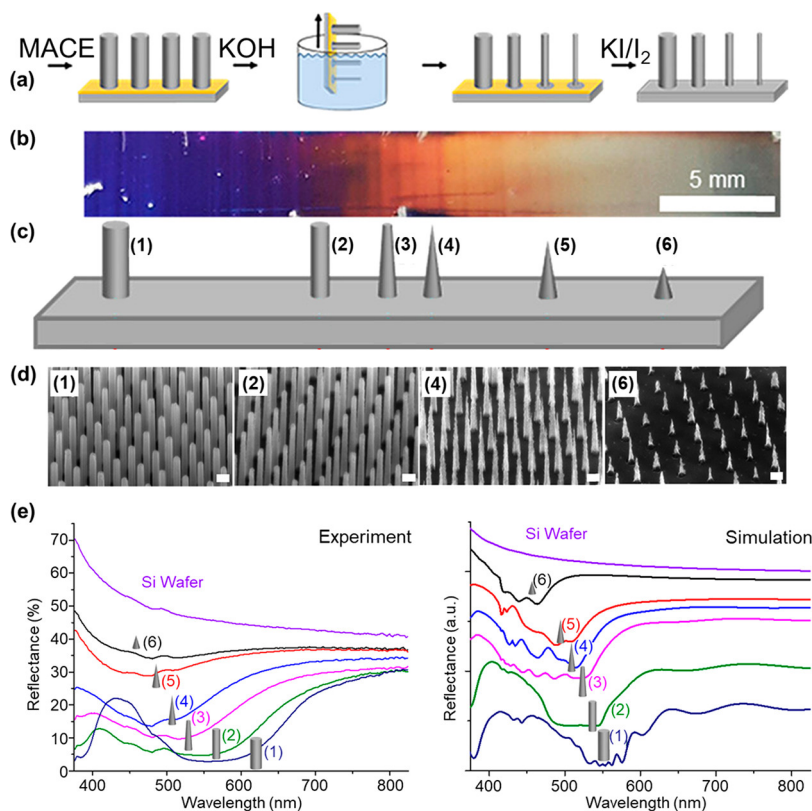


Figure 11. (a) Schematics showing the dip-etching process to fabricate gradient SiNWs (b) Optical image of a gradient SiNW sample. (c, d) Scheme of the gradient morphology at various positions indicated with numbers and corresponding electron SEM images at those positions. (e) Measured and simulated reflectance spectra for different positions on the SiNW structure.⁵³ Adapted with permission from ref 53. Copyright 2020 American Chemical Society.

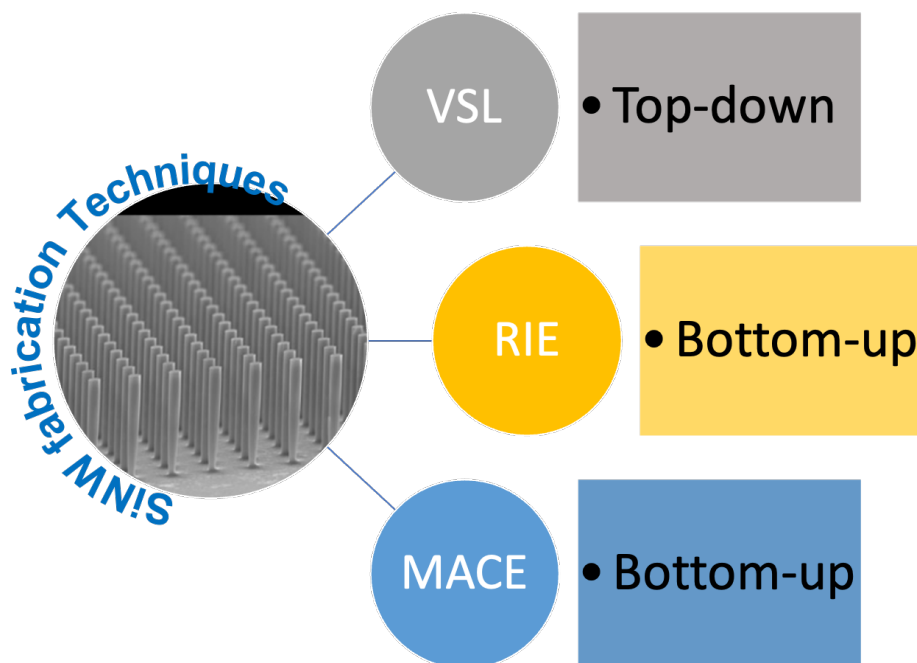


Figure 12. Summary of SiNW fabrication techniques

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